DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING, MIT MANIPAL

M.TECH. MICROELECTRONICS (ME)

Program Structure (Applicable to 2023 admission onwards)

YEAR	FIRST SEMESTER						SECOND SEMESTER					
	SUB CODE	**SUBJECT NAME**	**L**	**T**	**P**	**C**	**SUB CODE**	**SUBJECT NAME**	**L**	**T**	**P**	**C**
I	MAT 5131	Probability and Random Processes	3	1	0	4	ECE 5214	CMOS Mixed Signal Design	3	1	0	4
	ECE 5112	Digital VLSI Design	3	1	0	4	ECE 5215	Low Power VLSI Design	3	1	0	4
	ECE 5113	Processor Architecture and Applications	4	0	0	4	ECE ****	Program Elective-I	4	0	0	4
	ECE 5116	Analog And RF VLSI Design	3	1	0	4	ECE ****	Program Elective-II	4	0	0	4
	ECE 5117	Semiconductor Device Fabrication Technology	4	0	0	4	ECE ****	Program Elective-III	4	0	0	4
	HUM 5051	Research Methodology and Technical Communication*	1	0	3	-	*** ****	Open Elective	3	0	0	3
	ECE 5141	Digital VLSI Design Lab	0	0	6	2	HUM 5051	Research Methodology and Technical Communication*	1	0	3	2
	ECE 5143	Analog and RF VLSI Lab	0	0	3	1	ECE 5262	VLSI Physical Design Lab	0	0	6	2
	Total		**18**	**3**	**12**	**23**			**22**	**2**	**9**	**27**
	THIRD AND FOURTH SEMESTER											
II	ECE 6091	Project Work and Industrial Training							**0**	**0**	**0**	**25**

*TAUGHT IN BOTH SEMESTERS AND EVALUATED AND CREDITED IN THE SECOND SEMESTER

PROGRAM ELECTIVES		OPEN ELECTIVE	
COURSE CODE	**COURSE TITLE**	**COURSE CODE**	**COURSE TITLE**
ECE 5401	Advanced Digital Signal Processing	ECE 5301	ARM Processor and Application
ECE 5402	Advances in Circuit Elements	ECE 5302	Nano Electronics
ECE 5403	Analog VLSI For Signal Processing	ECE 5303	Neural Networks and Fuzzy Logic
ECE 5404	CAD For VLSI		
ECE 5405	Cryptography & Network Security		
ECE 5406	Communication Networks And Protocols		
ECE 5407	High Speed Digital Design		
ECE 5408	Large Area Micro Electronics		
ECE 5409	MEMS Technology		
ECE 5410	Microwave and Millimeter Wave Antenna		
ECE 5411	Nano - Photonics		
ECE 5412	Nonlinear Fiber Optics		
ECE 5413	Quantum Information Science		
ECE 5414	RF Microelectronics Chip Design		
ECE 5415	Spread Spectrum Communication		
ECE 5416	System On Chip Design		
ECE 5417	VLSI Physical Design and Verification		
ECE 5418	VLSI Testing & Testability		

SEMESTER I

MAT 5131 PROBABILITY AND RANDOM PROCESSES [3 1 0 4]

Stochastic Processes – types, fundamental concepts, limiting and transient behaviour. Poisson process – properties. Birth-death models, Queueing models-performance measures. Estimation-properties of estimators, methods of estimation, Time series models-linear and non-stationary processes.

*Self-Directed Learning: Fourier analysis of deterministic signals-DFT and periodogram, Spectral densities and representations, Wiener-Khinchin theorem, Harmonic processes, SARIMA models.

References:

1. Stewart, William J. Probability, Markov chains, queues, and simulation: the mathematical basis of performance modeling. Princeton university press, 2009.
2. Tangirala, Arun K. Principles of system identification: theory and practice. CRC Press, 2018.
3. U. Narayan Bhat, "An introduction to queueing theory: modeling and analysis in applications", Birkhäuser, 2015.
4. *Casella, George, and Roger L. Berger. Statistical inference. Cengage Learning, 2021.
5. A. Papoulis and S.U. Pillai, "Probability, Random Variables and Stochastic Processes", McGraw Hill, 2002.
6. *P. Z. Peebles Jr., "Probability, Random Variables and Random Signal Principles", McGraw Hill International Edition, 2001, Singapore.
7. * https://onlinecourses.nptel.ac.in/noc22_ch19/preview

ECE 5112 DIGITAL VLSI DESIGN [3 1 0 4]

MOS Transistor theory, Inverters, Combinational and Sequential Digital circuit design, VLSI Fabrication and Layouts, CMOS/Bulk technology, SOI technology. Basic circuit concepts and performance estimation; Design Margins and Reliability; Alternatives to CMOS Logic, BiCMOS logic; Subsystems design and Building Blocks; Semiconductor memories.

*Self-Directed Learning: Coping with interconnects in VLSI

References:

1. *Jan M, Rabaey, et al, Digital Integrated Circuits: A Design Perspective, Prentice Hall, 2003.
2. Neil Weste and K. Eshragian, Principles of CMOS VLSI Design: A System Perspective, Pearson Education, 2000.
3. Sung, Mo Kang and Yosuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, TMH, 2003
4. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design *PHI*, 2005.
5. Wayne, Wolf, Modern VLSI design: System on Silicon Pearson Education, 2005.

ECE 5113 PROCESSOR ARCHITECTURE AND APPLICATIONS [4 0 0 4]

Introduction, data path, control, pipelining. Building a Data path, a simple implementation scheme for R instructions, memory related, branch / jump instructions, ALU control, a multi cycle Implementation. Pipelining basics, hazards, pipelined data path and control, data hazards, forwarding, stalls, branch hazards, HDL model of a pipeline, advanced Pipelining, Pentium 4 pipelining. Basics of cache, cache architecture, cache optimization, MMU, programmed I /O, Interrupt I/O, DMA. Concepts of Instruction level parallelism & Challenges, dynamic Scheduling, advanced techniques for Instruction delivery and speculation, limitations of ILP. A taxonomy of parallel architectures, shared memory architectures, basics of cache coherence protocols, basics of Vector Processor, MSP 430 – Architecture, features. Basic architectural features of digital signal processors, computational building blocks, data representation and

arithmetic, finite word length effects, addressing modes, architecture of TMS 320C62x / 64x / 67x processor and its features, DSP development tools, Code Composer Studio & Simulink, applications of DSP Processors.
*Self-Directed Learning: Introduction to Code Composer Studio & Simulink

References:

1. David A. Patterson & John L. Hennessy, "Computer Organization and Design-The Hardware/Software Interface", ARM Edition, Elsevier, 2014.
2. John L. Hennessy and David A. Patterson, "Computer Architecture-A Quantitative Approach", Fourth Edition, Elsevier, 2007.
3. Phil Lapsley, "DSP Processor Fundamentals", IEEE Press, 1997.
4. Sen M. Kuo, Woon Seng Gan, "Digital Signal Processors", Pearson, 2005.
5. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide" Elsevier, 2004
6. * Texas Instruments Code Composer Studio https://www.ti.com/tool/CCSTUDIO

ECE 5116 ANALOG AND RF VLSI DESIGN [3 1 0 4]

Review of MOS device, Second-order effect, Long-channel and short-channel devices, Low-frequency and high-frequency MOS models, Noise, Analog Design flow, Design issues, Current sources and sinks; CMOS Amplifiers; Operational Trans conductance Amplifiers(OTA). Analog Layout considerations, CMOS RF Circuit Design, Frequency Synthesizers; Layout considerations for Analog and RF.
*Self-Directed Learning: Layout of Analog circuits

References:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill, 2002.
2. David A. Johns, Ken Martin, Analog Integrated Circuit Design, Johns Wiley & Sons, 2002.
3. R. Jacob Baker, Harry W. Li, David E. Boyce, CMOS circuit design, Layout, and Simulation, IEEE Press, PHI Pvt. Ltd, 1998.
4. Phillip. E. Allen, and Douglas R. Holberg, CMOS Analog Circuit Design, Second edition, Oxford University Press, 2004.
5. Thomas H. Lee, "Design of CMOS RF Integrated Circuits" Cambridge University, 2004.
6. * https://nptel.ac.in/courses/117/101/117101105/

ECE 5117 SEMICONDUCTOR DEVICE FABRICATION TECHNOLOGY [4 0 0 4]

Material Properties; Clean Room Technology and Silicon Wafer Production, Crystal Growth; Silicon Oxidation; Kinetics of Growth, Deal-Grove Model, lithography, Next generation lithography; Photoresist, Diffusion, ion stopping and channeling; etching, Metallization: Thin Film Deposition: Evaporation and Sputtering, Thin Film Deposition: Chemical Vapor Deposition, Epitaxy, Measurement techniques:
*Self-Directed Learning: Optical microscope, Scanning Electron Microscope, energy dispersive analysis of X-rays, Augur analysis, Secondary Ion Mass Spectroscopy (SIMS). Advanced technologies.

References:

1. *Stephen A. Campbell, The Science & Engineering of Microelectronic Fabrication, Second Edition, Oxford University Press, 2005.
2. Gary S. May and S. M. Sze, Fundamentals of Semiconductor Fabrication, Wiley Student edition, 2004.
3. James D. Plummer, Michael D. Deal and Peter B. Griffin Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson, 2000.
4. S.K. Gandhi, VLSI Fabrication Principles, John Wiley & Sons, 1983.
5. S. M. Sze, VLSI Technology, Second Edition, McGraw Hill, 1988.

HUM 5051 RESEARCH METHODOLOGY AND TECHNICAL COMMUNICATION [1 0 3 2]

Research Methodology: Basic concepts: Types of research, Significance of research, Research framework. Sources of data, Methods of data collection. Research formulation: Components, selection and formulation of a research problem, Objectives of formulation, and Criteria of a good research problem. Research hypothesis: Criterion for hypothesis construction, Nature of hypothesis, Characteristics and Types of hypothesis, Elements of research design, Introduction to various sampling methods Sources of data, Collection of data, Research reports, references styles, Effective Presentation techniques, Research Ethics.

References:

1. Sekaran, U., & Bougie, R. (2016). Research methods for business: A skill building approach. John Wiley & Sons.
2. Zikmund, W. G., Babin, B. J., Carr, J. C., & Griffin, M. (2013). Business research methods. Cengage Learning.
3. Creswell, J. W., & Creswell, J. D. (2017). Research design: Qualitative, quantitative, and mixed methods approaches. Sage Publications.
4. Donald R Cooper & Pamela S Schindler, Business Research Methods, McGraw Hill International, 2018.

ECE 5141 DIGITAL VLSI DESIGN LAB [0 0 6 2]

Introduction to ASIC Design flow using Cadence tool. RTL modelling of Combinational and Sequential Digital circuits using Verilog. Synthesise and Implement various logic circuits in Artix-7/Basys-3 FPGA boards. Synthesize Mealy and Moore FSMs to implement Algorithms. Functional verification of Digital Systems and memory using SystemVerilog. Synthesis of digital circuits in Cadence Genus tool using hardware aware HDL modelling, optimizing performance, power and area.

References:

1. Charles Roth, Lizy Kurian John, Byeong Kil Lee, Digital System Design Using Verilog, 1st Edition, 2016.
1. Samir Palnitkar, "Verilog HDL: a guide to digital design and synthesis", Prentice Hall Professional, 2003.
3. Ashok B Mehta, "Introduction to System Verilog", Springer, Netherlands, 2022.
4. Spear, Chris, "SystemVerilog for verification: a guide to learning the testbench language features" Springer Science & Business Media, 2008.
5. Digital Lab Manual, Revision 2.0, University Support Team, Cadence, Bengaluru, 2017.

ECE 5143 ANALOG AND RF VLSI LAB [0 0 3 1]

Introduction to Design and simulation of Analog circuits using Cadence software, Analysis and simulation of Basic and cascode current mirror circuit, Analysis and design of Wilson and wide swing cascode current mirror, Analysis and design of CS amplifier with different load, Analysis, and design of CD amplifier with different load, analysis, and design of the differential amplifier and Operational Transconductance Amplifier , Design, and simulation of RF blocks using Cadence software: RF-design-of-1.9-ghz-rx-front-end block: analysis of LNA, analysis, and design of gilbert cell, Quadrature oscillator Identify a research problem and develop a mini-project.

References:

1. Cadence Virtuoso User Manual.

2. R. Jacob Baker, Harry W. Li, David E. Boyce, CMOS circuit design, Layout, and Simulation, 3rd edition, IEEE Press, PHI Pvt. Ltd, 2010.
3. David A. Johns, Ken Martin, Analog Integrated Circuit Design, 2nd edition, Johns Wiley & Sons, 2013.
4. Philip E. Allen and Douglas Holberg, CMOS Analog Circuit design, Second Edition, Oxford University Press, 2012
5. Behzavi Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill Publishing Company Ltd., 2002.

SEMESTER II

ECE 5214 CMOS MIXED SIGNAL DESIGN [3 1 0 4]

Analog and Mixed-mode Building Blocks; current mode circuit design; Discrete-time Filters; Continuous-time (CT) Filters; Data Converters; Analog circuits for Sensor Interfacing Applications; Mixed Signal Layout Issues.
*Self-Directed Learning: Circuit analysis for Analog designers.

References:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill, 2002.
2. David A. Johns, Ken Martin, Analog Integrated Circuit Design, Johns Wiley & Sons, 2002.
3. R. Jacob Baker, Harry W. Li, David E. Boyce, CMOS circuit design, Layout, and Simulation, IEEE Press, PHI Pvt. Ltd, 1998.
4. Phillip. E. Allen, and Douglas R. Holberg, CMOS Analog Circuit Design, Second edition, Oxford University Press, 2004.
5. Thomas H. Lee, "Design of CMOS RF Integrated Circuits" Cambridge University, 2004.
6. * https://nptel.ac.in/courses/117106148/L01

ECE 5215 LOW POWER VLSI DESIGN [3 1 0 4]

Sources of power dissipation. Hierarchical Low Power Design Methodologies. Architecture Level Power reduction techniques; Switching activity reduction techniques; Interconnect Power; Sources of leakage in CMOS and Static Power reduction technique; Low power memory design; System level power reduction techniques.
*Self-Directed Learning: Power aware RTL coding.

References

1. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP, 2002.
2. *Christian Piguet, Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools, CRC press, 2005
3. Ajith Pal, Low-Power VLSI Circuits and Systems, Springer, 2015.
4. Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI Circuit Design Wiley, 2000.
5. Kiat Seng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Edition 2009, Tata Mc Graw Hill.

ECE 5262 VLSI PHYSICAL DESIGN LAB [0 0 6 2]

Introduction to VLSI Physical Design flow using Cadence tool. Plan the physical design of digital circuits using Cadence Innovus implementation system. Identify a research problem and develop a mini-project.

References:

1. Digital Lab Manual, Revision 2.0, University Support Team, Cadence, Bengaluru, 2017.

SECOND YEAR

ECE 6091 PROJECT WORK & INDUSTRIAL TRAINING [0 0 0 25]

Students are expected to work for about 40 to 50 weeks under a guide from the department on a project relevant to the curent research trends and/or to the industry requirements. The work is expected to showcase the knowledge gained by them through two semesters of coursework as well as through a literature survey pertaining to the project. The work can be carried out in the home institution, an industry, any research laboratory of repute, or other premier institutions.

References:

1. Lab manuals associated with EDA tools/Soft computing tools etc.
3. Company/Industry user manual and their internal document.
4. IEEE Xplore/Scopus/WOS Indexed Journal articles/review articles/case studies/conference proceedings etc.
5. Associated Reference books.

PROGRAM ELECTIVES

ECE 5401 ADVANCED DIGITAL SIGNAL PROCESSING [4 0 0 4]

Signals, Multi-rate Systems, Interpolated FIR Filters for Decimation and Interpolation Filters, Quadrature Mirror Filter Bank (QMF), Half band and multiband filters, PR systems. Principle of Adaptive filters, Tapped Delay Line and Weiner Filters, Steepest Descent Algorithm, LMS Algorithm. Homomorphic system, Complex Cepstrum, Hilbert transform, Homomorphic systems, applications. Discrete-time random processes, Signal modeling, Spectrum estimation.

References:

1. J. G. Proakis and D.G. Manolakis, Digital Signal Processing: Principles, Algorithms, and Applications, 4/e, *Pearson Education*, 2007.
2. P. P Vaidyanathan, Multirate Systems And Filter Banks, *Prentice Hall*, India,1993.
3. A.V Oppenheim.and R.W. Schafer, Digital Signal Processing, *Prentice Hall*, 1992.
4. S. J Orfanidis, Optimum Signal Processing, *Mc Graw Hill* , NJ ,2007.
5. M H Hayes, Statistical signal processing and modeling, *John Wiley &Sons*, Inc, 2002

ECE 5402 ADVANCES IN CIRCUIT ELEMENTS [4 0 0 4]

Fundamental circuit elements, Gyrator, Emulation of grounded and floating inductor, Emulation of negative circuit elements, New circuit elements: Frequency Dependent Negative Resistor, Constant Phase Element , Fractional Order Elements - Fractional Order Capacitor, Fractional Order Inductor, Memristor: modeling. Emulation and applications

References:

1. Georgia Tsirimokou, Costas Psychalinos, Ahmed Elwakil, Design of CMOS Analog Integrated Fractional-Order Circuits: Applications in Medicine and Biology, Springer, May 2017.
2. Aleksei Tepljakov, Fractional-order Modeling and Control of Dynamic Systems, Springer Thesis, 2017.
3. Vourkas, Ioannis, Sirakoulis, Georgios, Memristor Based Nanoelectronic Computing Circuits and Architectures, Springer Publishers, 2016.

4. Vaidyanathan, Sundarapandian, Volos, Christos, Advances in Memristors, Memristive Devices and Systems, Springer Publishers, 2017.
5. Biswas, K., Bohannan, G., Caponetto, R., Mendes Lopes, A., Tenreiro Machado, J.A., Fractional-Order Devices, Springer Publishers, 2017.

ECE 5403 ANALOG VLSI FOR SIGNAL PROCESSING [4 0 0 4]

Basic CMOS Circuit Techniques, Continuous- Time Signal Processing. Low Voltage Signal Processing. Current- Mode Signal Processing: Continuous- Time Signal Processing, Sampled-Data Signal Processing, Switched-Current Data Converters. Analog Filters. Statistical Modeling and Simulation, Correlations and Principal Component Analysis, Statistical device Modeling, Statistical Circuit Simulation, Analog Layout.

References:

1. Mohammed Ismail, Analog VLSI : Signal and Information Processing, McGraw-Hill, 1994.
2. R.Schaumann, M.S.Ghausi, Kenneth R Laker, Design of Analog Filters Passive, Active RC, and Switched Capacitor, Prentice Hall, 1995.
3. T Deliyanis, Y.Sun and J.K.Fidler, Continuous-Time Active Filter Design, CRC Press,1999.
4. P.V.Anand Mohan, Current-mode VLSI Analog Filters: Design and Applications, Birkhauser, 2003.

ECE 5404 CAD FOR VLSI [4 0 0 4]

Graph Theory, Graph optimization Problems and Algorithms. Programmable logic devices, FPGA Classification. Architectural Synthesis, Scheduling, Different types of scheduling with and without resource constraint algorithms. Two level combinational logic synthesis and optimization; Exact and heuristic method. Cell Library Mapping**.**

***Self-Directed Learning:** High level logic synthesis, Data flow graph - sequencing graph-nodes, terminals in sequencing graph, scheduled graph.

References:

1. *Giovanni De Michelli , Synthesis and Optimisation of Digital Circuits, Tata-McGraw Hill, New Delhi, 2008.
2. Gary D. Hachtel, Fabio Somenzi , Logic Synthesis and Verification Algorithm, Kluwer Academic Publication, Boston, 2002.
3. M. J. S. Smith , Application Specific ICs, Addison Wesley,2002.
4. Donald Givone, “Digital Principles and Design”, McGraw Hill Education, 2017.
5. Narsingh Deo, “Graph theory with application to Engineering and Computer Science”, prentice hall India, 2013.

ECE 5405 CRYPTOGRAPHY & NETWORK SECURITY [4 0 0 4]

Classical Encryption Techniques. Public-Key Cryptography and RSA. Key Management and Distribution: Wireless Network Security: Security Technology Firewalls and VPNs; Access control. Firewalls. Virtual Private Networks. Intrusion Detection and Prevention Systems. Honeypots, Honey-nets and Padded cell systems. Scanning and analysis tools. Biometric access controls

References:

1. William Stallings, Cryptography and Network Security, Pearson 6th edition. 2004
2. M. E. Whitman and Herbert J. Mattored, Principles of Information Security, Information Security Professional, Fourth edition. ,2011.
3 .K. Pachghare, Cryptography and Information Security. PHI Learning, 2015

ECE 5406 COMMUNICATION NETWORKS AND PROTOCOLS [4 0 0 4]

Network Services and Layered Architecture. Packet Switched Network. Asynchronous Transfer Mode: Classical IP over ATM. Wireless Networks: Wireless Channel: Path loss, fading, Inter symbol Interference, Doppler frequency shift, Capacity limits. Optical Networks. single hop and Multi hop LAN, SONET/SDH

References:

1. Jean Walrand, Pravin Varia, High Performance Communication Networks, 2nd edition, 2009.
2. Behrouz. A, Forouzan, Data Communication and Networking, Tata McGrawHill,2008
3. Albert Leon-Garcia, Indra Widjaja,Communication Networks: Fundamental Concepts and Key Architectures, Tata McGraw –Hill 2nd Edition, 2004
4. Sumit Kasera and Pankaj Sethi, ATM Networks Concept and Protocol, Tata McGraw Hill Publication, 2006.
5. Rajiv Ramaswami, Kumar N. Optical Networks, Morgan Kaufmann Publishers 2nd Edition, 2008.

ECE 5407 HIGH SPEED DIGITAL DESIGN [4 0 0 4]

High speed logic gates; Measurement Techniques. Transmission Lines: Shortcomings of ordinary point-to-point wiring, effects of source and load impedance, Ground Planes and Layer Stacking; Terminations and Vias; Power Systems: distribution problems. Connectors, Special Connectors, Ribbon Cable. Clock Distribution, Using canned clock oscillators, Clock jitter

References:

1. Howard Johnson, Martin Graham, High-Speed Digital Design, A handbook of black magic, Pearson Education, 2008.
2. Stephen H. Hall & Howard L. Heck, Advanced Signal Integrity for High-Speed Digital Designs, John Wiley & Sons, 2009
3. William J Dally & John W Poulton, Digital Systems Engineering, Cambridge University Press, 1998
4. Eric Bogatin, Signal and Power Integrity- Simplified, 2ndEdition, Prentice Hall, 2010

ECE 5408 LARGE AREA MICRO ELECTRONICS [4 0 0 4]

Non-crystalline semi-conductor basics, Difference between, amorphous, polycrystalline and micro /nano crystalline hydrogenated silicon (a-Si:H), Thin Film transistor, LEDs, Large Area Image Sensor Arrays, Thin Film Position Sensitive Detectors. Field emission displays. Introduction to organic semiconductors- structure and geometry, stretchable and conformal electronics.

References:

1. Richard Zallen, The Physics of Amorphous solids, Wiley, 2007.
2.. Sanjiv Sambandan, CIRCUIT DESIGN- Techniques for Non-Crystalline Semiconductors, CRC press, 2013.
3. Robert A. Street , Technology and Applications of Amorphous Silicon,. Springer-Verlag New York, LLC Series: Series in Materials Science, 2004.
4. A.Madan & M.P.Shaw , The Physics and Technology of Amorphous silicon, Elsevier Science & Technology books, 2012.
5. Takao Someya, Stretchable Electronics, Wiley-VCH; 1 Edition, January 29, 2013.

ECE 5409 MEMS TECHNOLOGY [4 0 0 4]

Background of MEMS, Bulk micromachining, surface micromachining, Micro-cantilevers, design of MEMS sensors, RF MEMS devises, Biosensors, MEMS device packaging

References:

1. Stephen D.Senturia Microsystem design , Kluwer Academic publications, 2001
2. Marc Madou, Fundamentals of Microfabrication, CRC Press, 1997
3. H. Bao, Micromechnanical Transducers: pressure sensors, accelerometers, and gyroscopes, Elsevier, NewYork 20004.
4. Gabriel M Rebeiz, RF MEMS Theory, design and technology. Wiley Inter science,2003
5. Sergey Y.Yurish, Mearia Teresa S.R.Gomes, Smart sensors and MEMS, Kluwer Academic Publishers, 2003

ECE 5410 MICROWAVE AND MILLIMETER WAVE ANTENNA [4 0 0 4]

Millimeter Wave Technology, Microwave and Millimeter Wave Systems, Guiding Structures, Metamaterials. Millimeter Wave Antennas: Path Loss and Antenna Directivity, Antenna Beam width, Maximum Possible Gain-to-Q, Polarization, Beam Steering Antenna, Millimeter Wave Design Consideration, Millimeter Wave Propagation, Fifth-generation systems

References:

1. Duixian Liu, Ulrich Pfeiffer, Janusz Grzyb and Brian Gaucher, Advanced Millimetre-wave Technologies: Antennas, Packaging and Circuits , Wiley, 2009
2. Sergey M. Smolskiy, Leonid A. Belov and Victor N. Kochemasov, Handbook of RF, Microwave, and Millimetre-Wave Components, Artech House Microwave Library, 2013
3. Kao-Cheng Huang, Zhaocheng Wang, Millimetre Wave Communication Systems, Wiley, 2011
4. Shiban K. Koul, Millimetre Wave and Optical Dielectric Integrated Guides and Circuits, Wiley-Inter **science**, 1st edition, 200.
5. David M. Pozar, Microwave and RF Design of Wireless Systems, Wiley, 2000.

ECE 5411 NANO PHOTONICS [4 0 0 4]

Light generation by nanostructures, semiconductor quantum wells, nanocrystals, nanowires. Light propagation in nanostructures, Photonic crystals, dielectric periodic structures. Surface Plasmon, transmission through subwavelength hole, subwavelength waveguides. Near-field optics, Nano-photonics.

References:

1. Lukas Novotny and Bert Hecht, Principles of Nano-Optics, *Cambridge University Press, 2012.*
2. Herve Rigneault, Jean-Michel Lourtioz, Claude Delalande and Juan Ariel Levenson, Nanophotonics, *Wiley, 2006.*

3. Mark L. Brongersma and Pieter G. Kik, Surface Plasmon Nanophotonics, *Springer, 2006.*
4. P.N. Prasad, Nanophotonics, *Wiley-Interscience, 2003*
5. John D. Joannopoulos, Robert D. Meade and Joshua N. Winn, Photonic Crystals, *MIT Press, 2007*

ECE 5412 NONLINEAR FIBER OPTICS [4 0 0 4]

Nonlinear optical effects in crystals. Pulse propagation through optical fibers. Third order dispersion, dispersion management. SPM induced spectral broadening, higher order nonlinear effects, optical solitons, XPM. Stimulated Raman and Brillouin scattering. Parametric processes.

References:

1. G. P. Agarwal, Nonlinear Fiber Optics, *Academic Press*, 2007.
2. A. Yariv and P. Yeh, Photonics: Optical Electronics in Modern Communications, *Oxford University Press*, 2007

3. G. P. Agarwal, Applications of Nonlinear Fiber Optics, *Academic Press* 2008.
4. R. W. Boyd, Nonlinear Optics, *Academic Press* 2008

ECE 5413 QUANTUM INFORMATION SCIENCE [4 0 0 4]

Classical Computation, Turing Machines and Circuits, Information, Erasure, Reversibility. Single Quantum Bits. Multiple Quantum Bits, Entanglement. Measurements, EPR-Bell Theorem. Quantum Transformations: Reversible Gates, Quantum Circuit Model. Quantum Algorithms: Deutch-Jozsa's and Simon's Problems, Subsystems. Error Corrections.

References:

1. Eleanor Rieffel and Wolfgang Polak, Quantum Computing: A Gentle Introduction, *MIT Press, 2014 (Paperback edition).*
2. Giuliano Benenti, Giulio Casati, and Giuliano Strini, Principles of Quantum Computation and Information, Volumes I and II, *World Scientific, 2004*.
3. Kaye, Laflamme, and Mosca, An Introduction to Quantum Computing, *Oxford University Press, 2007*.
4. Nielsen and Chuang, Quantum Computation and Quantum Information, 10th *Anniversary Edition, Cambridge University Press, 2011*.

ECE 5414 RF MICROELECTRONICS CHIP DESIGN [4 0 0 4]

RF circuit design, Basic RF modules, Passive and active RF components, RF power amplifier, impedance matching, low noise amplifier (LNA), RF Filters, oscillators, mixers, modulators, detectors, and synthesizers.

References:

1. Thomas H. Lee Design of CMOS Radio-Frequency Integrated Circuits Cambridge University press, 2003.
2. Behzad Razavi RF Microelectronics, Prentice Hall International **Publisher,** 1998.
3. W. Alan Davis, Krishna K. Agarwal, Radio Frequency Circuit Design, John Wiley & Sons Inc., 2001.
4. Cotter W. Sayre, Complete Wireless Design, McGraw-Hill Professional Publisher, 2008.
5. John M. W. Rogers, John W. M. Rogers, Calvin Plett , Radio Frequency Integrated Circuit Design , Artech House Publishers, 2010.

ECE 5415 SPREAD SPECTRUM COMMUNICATION [4 0 0 4]

Direct sequence and frequency hop spread spectrum systems. Hybrid direct sequence/frequency hop spread spectrum. Sequence generators. Spread spectrum communication system model, diversity reception in fading channels, cellular radio concept, single and multicarrier CDMA.

References:

1. R. L. Peterson, R. E. Zeimer and D. E. Borth, Introduction to Spread Spectrum Communications, Pearson, 1995.
2. J. D. Proakis and M. Salehi, Digital Communication, McGraw Hill, 2008.
3. A. J. Viterbi, CDMA: Principles of Spread Spectrum Communications, Addision Wesley, 1995.
4. S. Verdu, Multiuser Detection, Cambridge University Press, 1998

ECE 5416 SYSTEM ON CHIP DESIGN [4 0 0 4]

SoC architecture, design issues; SoC design flow; logic cores, memory and analog cores; Design validation, Testing, embedded memories, analog and mixed signal core. Low power

architecture, Subsystem design principles, Floor planning, Off- chip connections, RTL design, High level synthesis, System on –chips Embedded CPUs, Hardware/ Software Co –Design.

References:

1. Rochit Rajsuman, System –on –a –Chip Design and test, Artech House, Bosten , London, ed., 2000
2. Peter J. Ashenden, Jean P. Mermet, Ralf Seepold, System-on-chip methodologies & design languages, Boston: Kluwer Academic Publishers, 2001
3. Wayne Wolf, Modern VLSI Design: System –on- Chip Design, Pearson, 2005
4. Michael Keating, Pierre Bricaud, Reuse methodology manual for system-on-a-chip designs, Boston: Kluwer Academic Publishers, 2001
5. Steve Furber, ARM System-on-Chip Architecture, 2nd Edition, Additon-Wesley professional, 2001.

ECE 5417 VLSI PHYSICAL DESIGN AND VERIFICATION [4 0 0 4]

Types of ASICs, ASIC/FPGA design flow, Logic Effort, library cell design, Timing Analysis-Static Timing Analysis, Introduction to Physical design, Physical design cycle, Partitioning, floorplanning, Pin assignment, Placement and Routing, Algorithms for physical design automation. Clock tree Synthesis, clock skew and power grid analysis, Power and ground routing, Cross talk, and reliability issues.

Introduction to Verification, Testing Vs Verification, the basic verification principle, and Verification methodology. Hardware Design Verification, Functional Verification, Formal method-based verification, Simulation-based verification, Equivalence checking: combinational and sequential systems, Verilog Scheduling and Execution Semantics, Simulator architectures. Introduction to SystemVerilog (SV)- Data Types & Procedural statements, Basic OOP, Randomization, Assertion, and Coverage. Connecting Test bench and Design.

*Self-Directed Learning: Universal Verification Methodology

References:

1. M. J. S Smith, “Application Specific Integrated Circuits” Pearson India, 1st edition, 2002.
2. N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective” Pearson, 4th edition, 2010.
3. S. Sait and H. Youssef “VLSI Physical Design Automation: Theory and Practice”, World Scientific, 1999.
4. William K. Lam, “Hardware Design Verification: Simulation and Formal Method-Based Approaches, Prentice hall PTR, 2005.
5. Ashok B Mehta, “Introduction to System Verilog”, Springer, Netherlands, 2022.
6. Chris Spear, “SystemVerilog for Verification: A Guide to Learning the Testbench Language Features”, Springer, 2010.
7. *SIEMENS | Verification Academy https://verificationacademy.com/courses/uvm-basics

ECE 5418 VLSI TESTING & TESTABILITY [4 0 0 4]

Digital and analog testing, Controllability and observability, Design-for-test, Test process and ATE, Fault modeling. Testing of combinational and sequential circuits. Test optimization and fault coverage. Testability - adhoc and structured approaches, Boundary scan. Signatures and Built-in self test, Reed-Muller and spectral coefficients, Signature analysis and Online self test.

*Self-Directed Learning: Power and Thermal Aware Test: Low power BIST, Thermal aware techniques.

References:

1. M. Abramovici, M. A. Breuer, and A.D. Friedman, "Digital Systems Testing and Testable Design", Piscataway, New Jersey: IEEE Press, 1994.
2. M. L. Bushnell and V. D. Agrawal, "Essentials of testing for digital, memory and mixed-signal VLSI circuits", Boston: Kluwer Academic Publishers, 2000.
3. Miczo, "Digital Logic Testing and simulation". New York: Harper & Row, 1986.
4. Krstic and K-T Cheng, "Delay Fault Testing for VLSI Circuits", Kluwer Academic Publishers, 1998.
5. P.K. Lala, "Fault Tolerant & Fault Testable hardware Design", BS Publications, 1998
6. Stanley L. Hurst, "VLSI Testing: digital and mixed analogue digital techniques" Pub:Inspec/IEE, 1999.
7. * https://www.digimat.in/nptel/courses/video/117105137/L39.html

OPEN ELECTIVES

ECE 5301 ARM PROCESSOR AND APPLICATION [3 0 0 3]

ARM embedded systems, Processor Fundamentals, Instruction Set, and Thumb Instruction Set. Assembler directives, Assembly coding, Memory System, MMU, Protection unit, Interrupts and Exceptions. ARM system architecture, AMBA Architecture, JTAG, Cortex-M3 architecture, OS support features; fault handling; Programming with Real time operating systems, Application programming. Programming with FreeRTOS.

Self-directed Learning: Programming with free RTOS

References:

1. Andrew Sloss, Dominic Symes, Chris Wright, ARM System Developer's Guide : Designing and Optimizing System Software, Elsevier, Morgan Kaufmann publisher, 2004.
2. Steve Furber, ARM System-on-Chip Architecture, 2nd Edition, Additon-Wesley professional, 2001.
3. Joseph Yiu, The Definitive Guide to the ARM Cortex-M0, Elsevier, Newnes, 2011.
4. Dr Alexander G. Dean, Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers: A Practical Approach, ARM Education Media, 2017.
5. Qing Li, Real time concepts for Embedded Systems, CMP Books, Elsevier, 2003
6. Richard Barry, Mastering the Free RTOS Real Time Kernel: A Hands on Tutorial Guide, 2016
7. https://www.freertos.org/

ECE 5302 NANO ELECTRONICS [3 0 0 3]

Nanomaterials, Nanostructured materials, Capabilities, physical fundamentals. Scaling principles, limits to scaling, power constrained scaling limits. Electronic transport in 1,2 and 3 dimensions- Quantum confinement. Electronic and optoelectronic properties of molecular materials. Spin tunneling devices, Ferroelectric random access memory, semiconductor sensor array. Nanotechnology for biological system & bio-sensor applications.

References:

1. V. Mitin, V. Kochelap, M. Stroscio, Introduction to Nano-electronics, Cambridge University Press, 2008.
2. Rainer Waser,Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley-VCH,2003.
3. Karl Goser, Peter Glosekotter, Jan Dienstuhl, Nano-electronics and Nano-systems, Springer, 2004.
4. Sadamichi Maekawa, Concepts in Spin Electronics, Oxford University Press, 2006.

5 Edward L. Wolf, Nanophysics and Nanotechnology: An Introduction to Modern Concepts in Nanoscience‖, Wiley-VCH, 2006.

ECE 5303 NEURAL NETWORKS & FUZZY LOGIC [3 0 0 3]

Biological neurons, Mc-culloch Pitt's model, Feed forward and Feedback network, Supervised and unsupervised learning. learning rules. Classifiers; Discrete time and gradient type, Hopfield networks, Unsupervised learning methods; cluster discovery network, Counter propagation networks. kernel methods. Fuzzy Logic: fuzzy systems, membership functions, classical sets and fuzzy sets, fuzzy set rules. Fuzzy relations, Approximate reasoning. Fuzzy inference engine, Fuzzifiers, Defuzzifiers, Neuro fuzzy systems, with GA optimization

References:

1. Jacek M Zurada, Introduction to artificial Neural Systems, Jaico publication. 2006
2. Simon Haykin, Neural Networks and Learning Machines, PHI edition private Limited,3rd edition, New Delhi, 2009
3. Li Xin Wang, Introduction to fuzzy systems and control, Prentice Hall publication, 1997
4. Timothy J Ross, Fuzzy Logic with Engineering Applications, Intl. Edition, McGraw Hill publication, 2008